

**AMENDMENTS TO THE CLAIMS**

1. (original) A semiconductor apparatus, comprising:  
  
a semiconductor substrate;  
  
an electrode pad including a metal layer and formed on the semiconductor substrate;  
  
a MOS transistor formed on the semiconductor substrate; and  
  
an analog circuit formed in a region under the electrode pad on the semiconductor substrate and comprising a resistive element including a semiconductor material.
2. (original) A semiconductor apparatus according to Claim 1, wherein the resistive element includes a specific material made of one of polysilicon, silicon germanium, and silicon chrome.
3. (original) A semiconductor apparatus according to Claim 1, wherein the resistive element includes a plurality of resistors.
4. (original) A semiconductor apparatus according to Claim 1, wherein the MOS transistor comprises a gate electrode including the specific material of the resistive element.
5. (original) A semiconductor apparatus according to Claim 1, further comprising:

an insulating film formed on the semiconductor substrate in a region in a vicinity of the electrode pad; and

a fuse element formed on the insulating film.

6. (currently amended) A semiconductor apparatus according to Claim ~~4~~ 5, wherein the insulating film includes the specific material of the resistive element.

7. (currently amended) A semiconductor apparatus according to Claim ~~4~~ 5, further comprising:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad.

8. (original) A semiconductor apparatus according to Claim 5, wherein the analog circuit comprises a voltage setting circuit, the resistive element comprises at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

9. (original) A semiconductor apparatus according to Claim 1, wherein the resistive element comprises at least two resistors for producing a split voltage based on an input source power voltage, the analog circuit comprises a reference voltage generator for generating a reference voltage and a voltage detector including a comparator for performing a comparison of the split voltage with the reference voltage.

10. (currently amended) A semiconductor apparatus according to Claim 1, wherein the analog circuit further comprises an output driver for controlling an output voltage based on an input voltage, and the comparator of the voltage detector outputs a gate control voltage as a result of the comparison for controlling the output driver to control the output voltage.

11. (currently amended) A method of manufacturing a semiconductor apparatus including a MOS transistor and an analog circuit having a resistive element including a semiconductor material, the method comprising the steps of:

providing a semiconductor substrate;

forming an insulating film on the semiconductor substrate;

forming a semiconductor material film on an entire surface of the semiconductor substrate including a formation region of the insulating film;

implanting an impurity ~~to~~ in the semiconductor material film to acquire a predetermined resistance value;

forming a resistive element on the insulating film by patterning the semiconductor material film;

forming a first insulating layer on an entire surface of the semiconductor substrate including a formation region of the resistive element; and

forming an electrode pad including a metal layer on the first insulating layer including ~~[[a]]~~ the formation region of the resistive element.

12. (original) A method according to Claim 11, wherein the resistive element includes a specific material made of one of polysilicon, silicon germanium, and silicon chrome.

13. (original) A method according to Claim 11, wherein the step of forming the resistive element forms the resistive element in a predetermined formation region of the resistive element and the resistive element includes a plurality of resistors.

14. (original) A method according to Claim 11, further comprising the steps of:

forming a second insulating layer having an opening at a position corresponding to a formation region of the electrode pad after the step of forming the electrode pad;

forming a rerouting layer on the electrode pad and the second insulating layer; and

forming an external connection terminal on the rerouting layer in a region different from the formation region of the electrode pad.

15. (original) A method according to Claim 11, wherein the step of forming the resistive element forms a gate electrode on the insulating film in a formation region of the MOS transistor based on the semiconductor material film.

16. (original) A method according to Claim 11, wherein the step of forming the resistive element forms a fuse element on the insulating film in a region

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different from the formation region of the resistive element based on the semiconductor material film.

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**AMENDMENTS TO THE DRAWINGS**

The attached replacement sheets of drawings includes changes to Figures 7 and 15.

Attachment: Replacement sheet